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Question Paper Code : 11382

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2012.

Sixth Semester

Electrical and Electronics Engineering

EC 1354 — VLSI DESIGN

(Common to Electronics and Communication Engineering)

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Design a NOR gate using basic CMOS technology.

2. Write a note on channel–length modulation.

3. How do the problem of latch up prevented?

4. Write a brief note on transmission gates.

5. What is the link between the shapes and resistances?

6. When the MOS characteristics is in the stage of accumulation, depletion and inversion, draw the capacitance effect.

7. Write a brief note on two phase clocking.

8. Design a simple half adder circuit.

9. What is the function of assert statement?

10. What is meant by overloading?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Discuss in detail the behavior of NMOS devices under the influence of different terminal voltages? (8)

(ii) Derive an expression for Threshold voltage. (8)

Or

(b) (i) Give a brief note on

(1) Body effect

(2) Mobility variation

(3) Fowler – Nordhum Tunneling

(4) Impact Ionization. (10)

(ii) Derive and draw the necessary equations for a small signal model of an MOS transistor. (6)

12. (a) Discuss in detail the characteristics of CMOS INVERTER circuit. Also draw the layout diagram and stick diagram for an inverter.

Or

(b) Write a detailed note on the following

(i) Pseudo – NMOS Inverter

(ii) Saturated load inverter

(iii) Cascode inverter

(iv) TTL interface inverter (5 + 5 + 3 + 3)

13. (a) With equation and necessary diagram explain in detail the capacitance estimation of MOS Device. (16)

Or

(b) For a CMOS inverter, draw the equivalent circuit and obtain.

(i) Fall delay

(ii) Rise time

(iii) Delay time

(iv) Gate delay

(v) Switch level RC model.

14. (a) Design the following circuits using VLSI design.

(i) Multiplexers

(ii) Multiplier

(iii) Full adder. (5 + 6 + 5)

Or

(b) Draw a neat layout, circuit diagram and explain with necessary equations for the following circuit.

(i) Bit serial adder

(ii) Carry save adder

(iii) Transmission gate adder

(iv) Carry look ahead adder.

15. (a) Discuss elaborately the various data types with example.

Or

(b) Explain in detail the various levels of modeling with suitable example.
